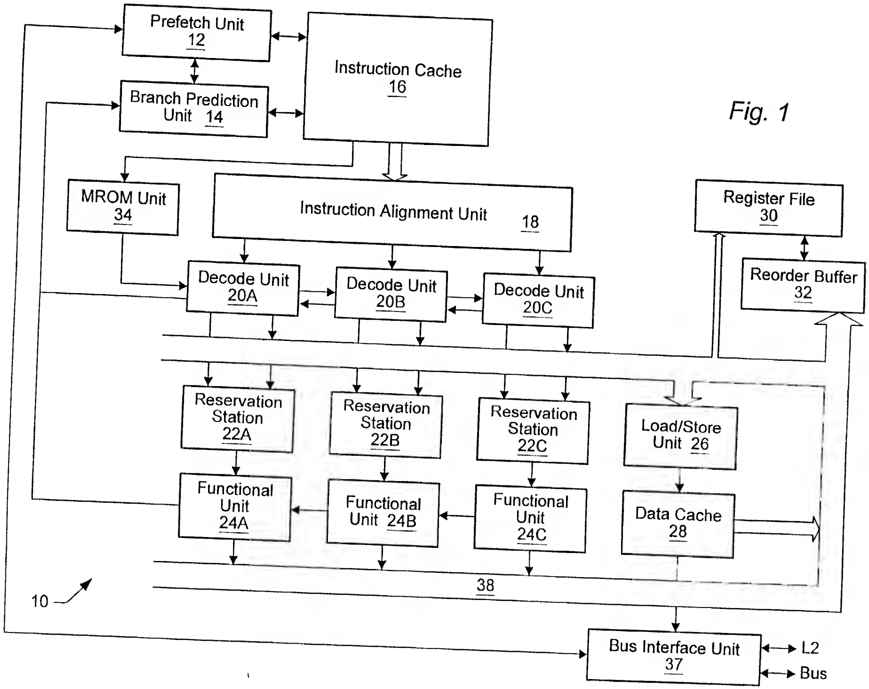

Prefetch Unit 12
Instruction Cache 16
Branch Prediction Unit 14
MROM Unit 34
Instruction Alignment Unit 18
Register File 30
Reorder Buffer 32
Decode Unit 20A
Decode Unit 20B
Decode Unit 20C
Reservation Station 22A
Reservation Station 22B
Reservation Station 22C
Load/Store Unit 26
Functional Unit 24A
Functional Unit 24B
Functional Unit 24C
Data Cache 28
38
10
Bus Interface Unit 37
L2
Bus

Fig. 1

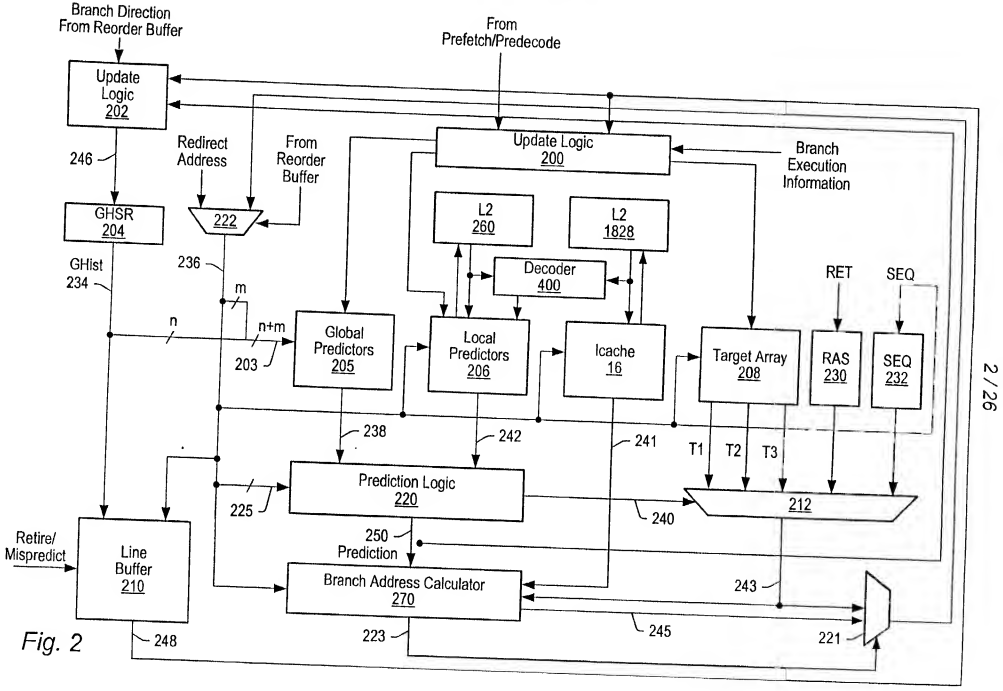


Fig. 2

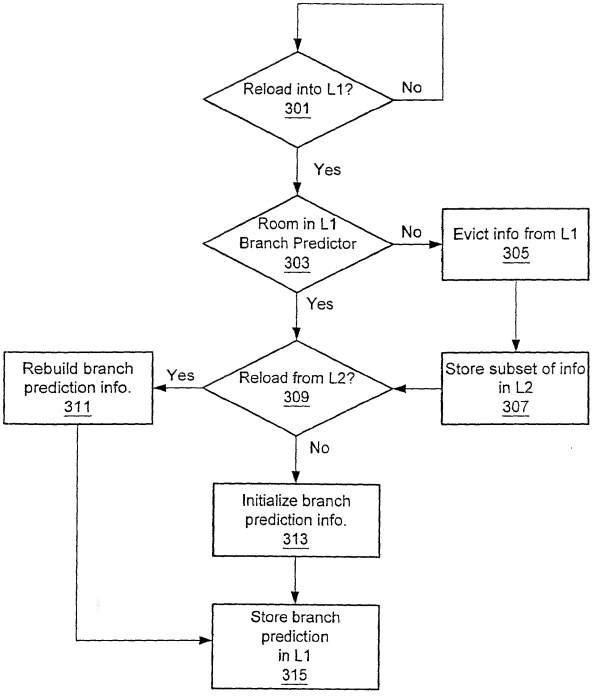

Reload into L1?
301
No
Yes
Room in L1 Branch Predictor
303
No
Evict info from L1
305
Yes
Rebuild branch prediction info.
311
Yes
Reload from L2?
309
Store subset of info in L2
307
No
Initialize branch prediction info.
313
Store branch prediction in L1
315

Fig. 3

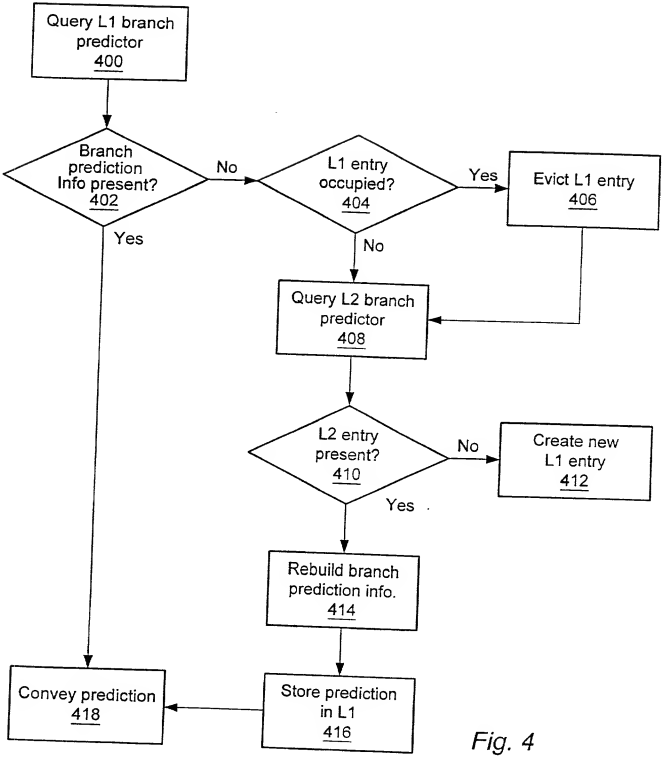

Query L1 branch predictor 400
Branch prediction Info present? 402
No
L1 entry occupied? 404
Yes
Evict L1 entry 406
Yes
No
Query L2 branch predictor 408
L2 entry present? 410
No
Create new L1 entry 412
Yes
Rebuild branch prediction info. 414
Store prediction in L1 416
Convey prediction 418

Fig. 4

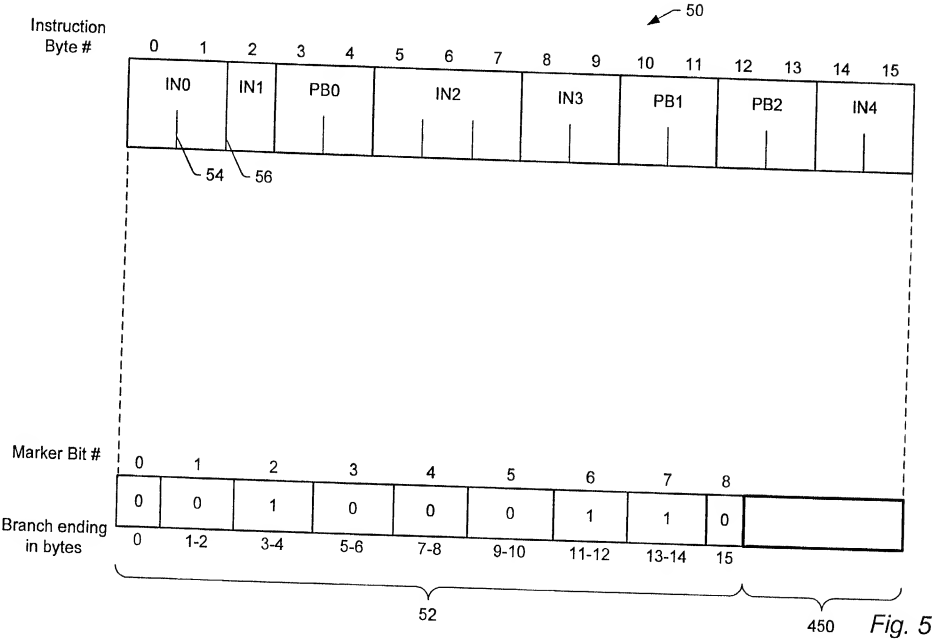
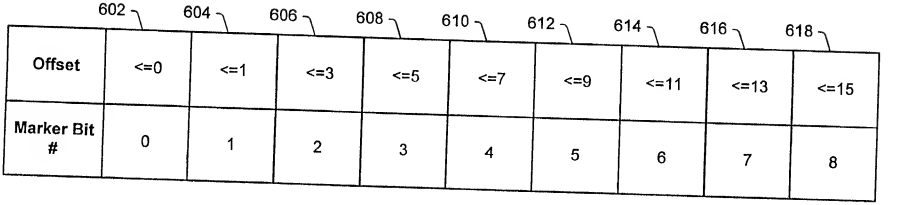

50
Instruction Byte #
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
IN0
IN1
PB0
IN2
IN3
PB1
PB2
IN4
54
56
Marker Bit #
0 1 2 3 4 5 6 7 8
0 0 1 0 0 0 1 1 0
Branch ending in bytes
0 1-2 3-4 5-6 7-8 9-10 11-12 13-14 15
52
450

Fig. 5



	602	604	606	608	610	612	614	616	618
Offset	<=0	<=1	<=3	<=5	<=7	<=9	<=11	<=13	<=15
Marker Bit #	0	1	2	3	4	5	6	7	8

Fig. 6

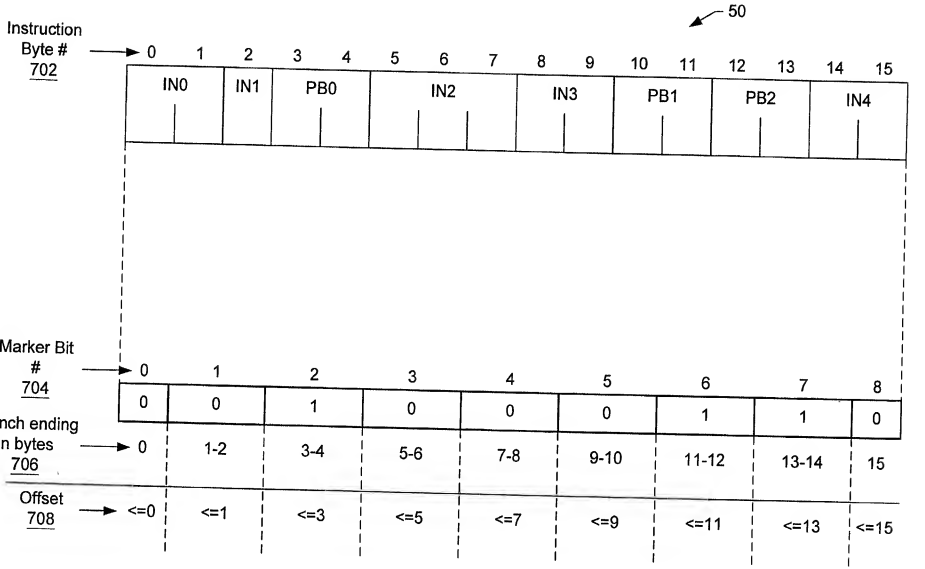

50
Instruction Byte # 702
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
IN0
IN1
PB0
IN2
IN3
PB1
PB2
IN4
Marker Bit # 704
0 1 2 3 4 5 6 7 8
0 0 1 0 0 0 1 1 0
Branch ending in bytes 706
0 1-2 3-4 5-6 7-8 9-10 11-12 13-14 15
Offset 708
<=0 <=1 <=3 <=5 <=7 <=9 <=11 <=13 <=15

Fig. 7

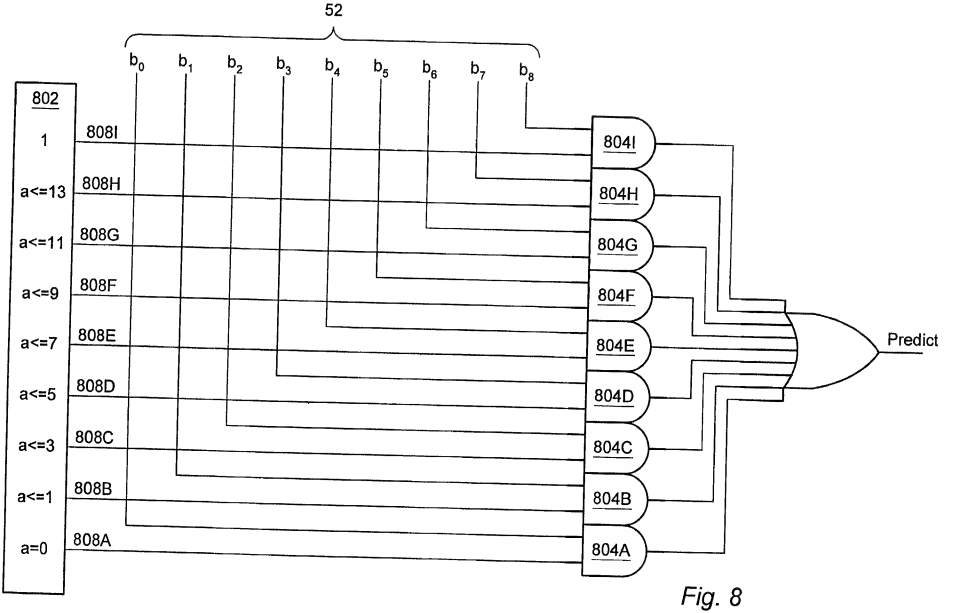

52
b_0 b_1 b_2 b_3 b_4 b_5 b_6 b_7 b_8
802
1
a<=13
a<=11
a<=9
a<=7
a<=5
a<=3
a<=1
a=0
808I
808H
808G
808F
808E
808D
808C
808B
808A
804I
804H
804G
804F
804E
804D
804C
804B
804A
Predict

Fig. 8

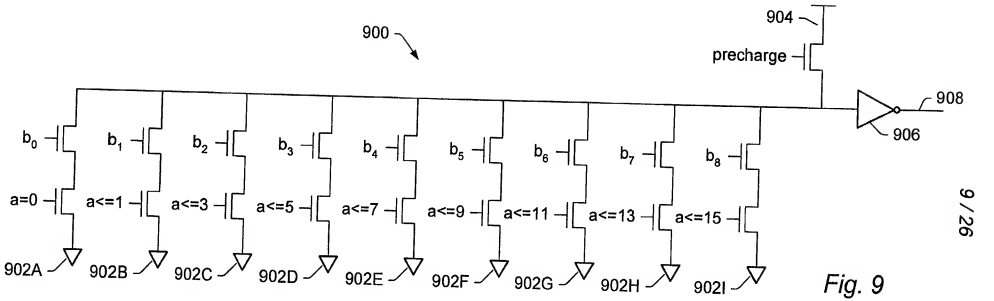

900
904
precharge
908
906
b_0
b_1
b_2
b_3
b_4
b_5
b_6
b_7
b_8
a=0
a<=1
a<=3
a<=5
a<=7
a<=9
a<=11
a<=13
a<=15
902A
902B
902C
902D
902E
902F
902G
902H
902I

Fig. 9

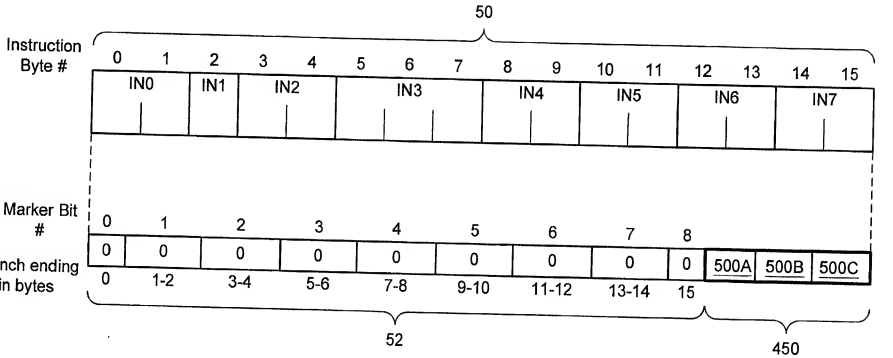

50
Instruction Byte #
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
IN0
IN1
IN2
IN3
IN4
IN5
IN6
IN7
Marker Bit #
0 1 2 3 4 5 6 7 8
Branch ending in bytes
0 0 0 0 0 0 0 0 0
500A
500B
500C
0 1-2 3-4 5-6 7-8 9-10 11-12 13-14 15
52
450

Fig. 10

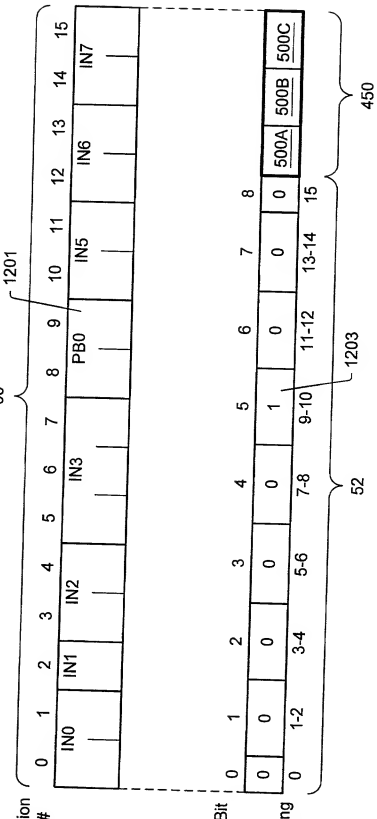

Instruction Byte #
Marker Bit #
Branch ending in bytes
50
52
450
1201
1203
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
IN0
IN1
IN2
IN3
PB0
IN5
IN6
IN7
0
1-2
3-4
5-6
7-8
9-10
11-12
13-14
500A
500B
500C

Fig. 11

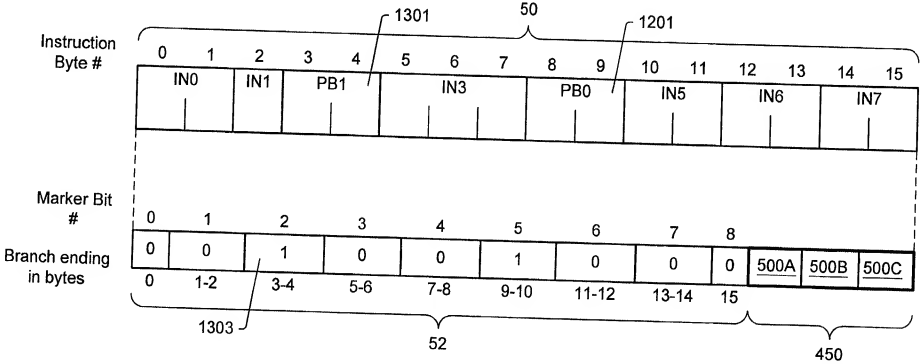


Fig. 12

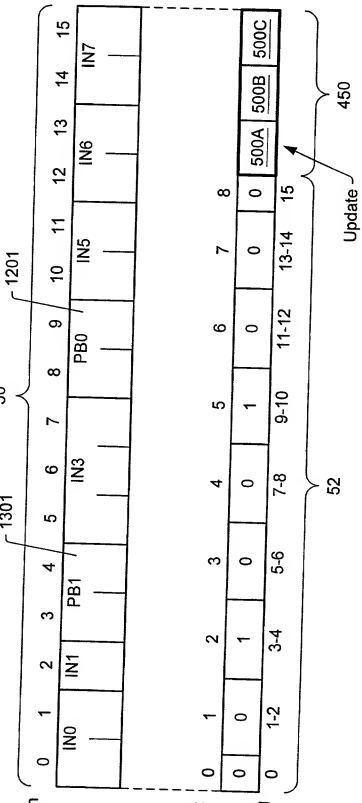

Instruction Byte #
Marker Bit #
Branch ending in bytes
50
52
1201
1301
450
Update
IN0
IN1
PB1
IN3
PB0
IN5
IN6
IN7
500A
500B
500C
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
0 0 1 0 0 1 0 0 0 0
0 1-2 3-4 5-6 7-8 9-10 11-12 13-14 15

Fig. 13

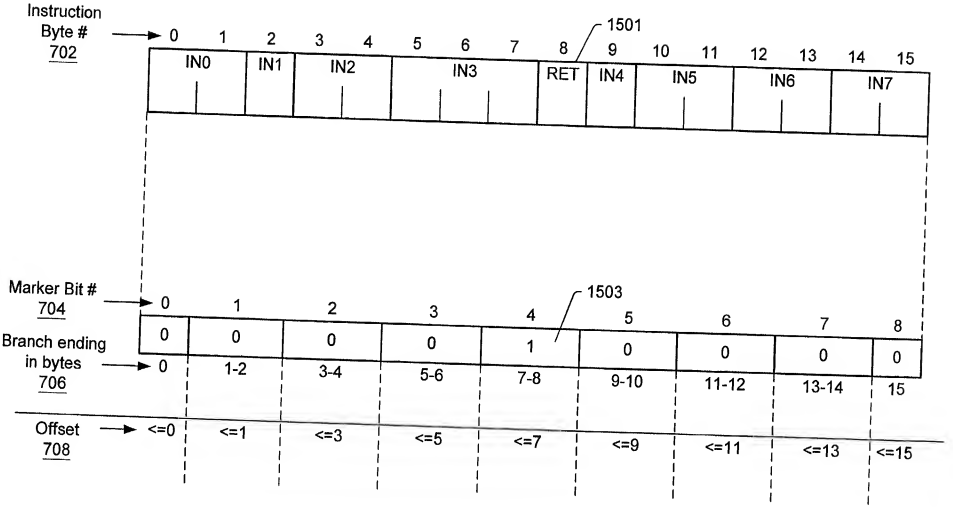

Instruction Byte # 702
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
1501
IN0
IN1
IN2
IN3
RET
IN4
IN5
IN6
IN7
Marker Bit # 704
0 1 2 3 4 5 6 7 8
1503
Branch ending in bytes 706
0 0 0 0 1 0 0 0 0
0 1-2 3-4 5-6 7-8 9-10 11-12 13-14 15
Offset 708
<=0 <=1 <=3 <=5 <=7 <=9 <=11 <=13 <=15

Fig. 14

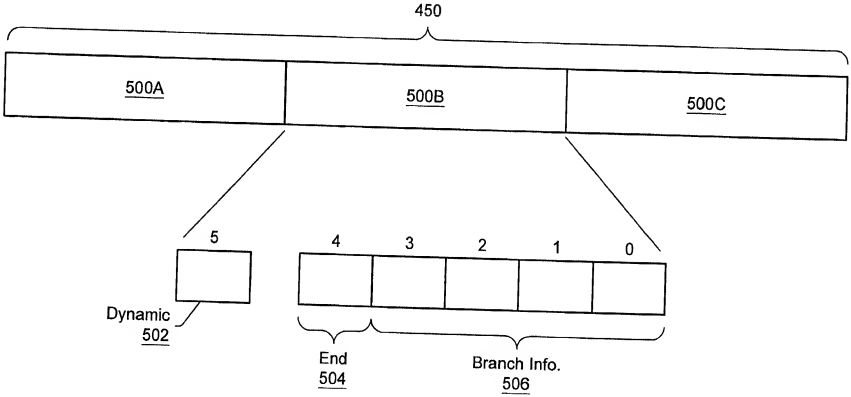

450
500A
500B
500C
5
Dynamic
502
4
3
2
1
0
End
504
Branch Info.
506
4
3
2
1
0
jcc
end
0
0
size
508
call
end
0
1
size
510
ret
end
1
0
0
0
512
C3
end
1
even position
514

Fig. 15

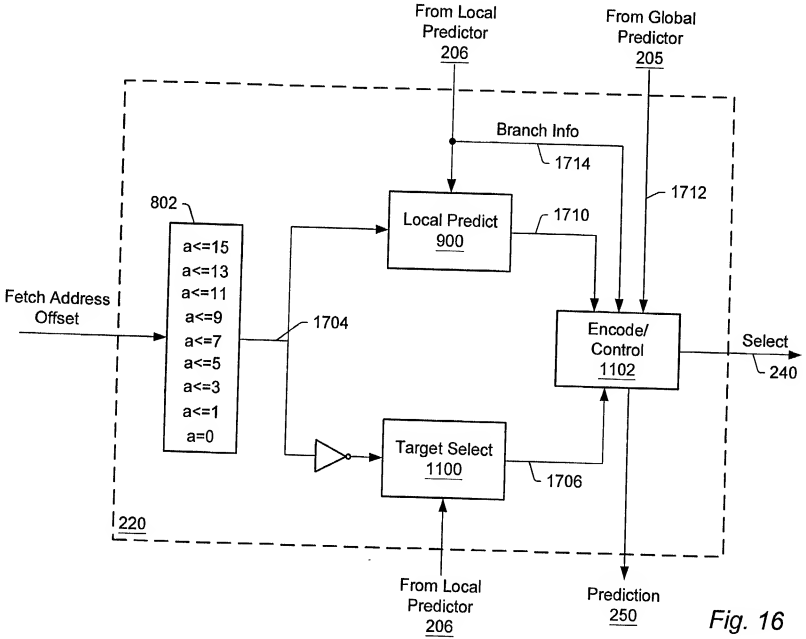

From Local Predictor 206
From Global Predictor 205
Branch Info
1714
1712
802
a<=15
a<=13
a<=11
a<=9
a<=7
a<=5
a<=3
a<=1
a=0
Local Predict 900
1710
Fetch Address Offset
1704
Encode/ Control 1102
Select
240
Target Select 1100
1706
220
From Local Predictor 206
Prediction 250

Fig. 16

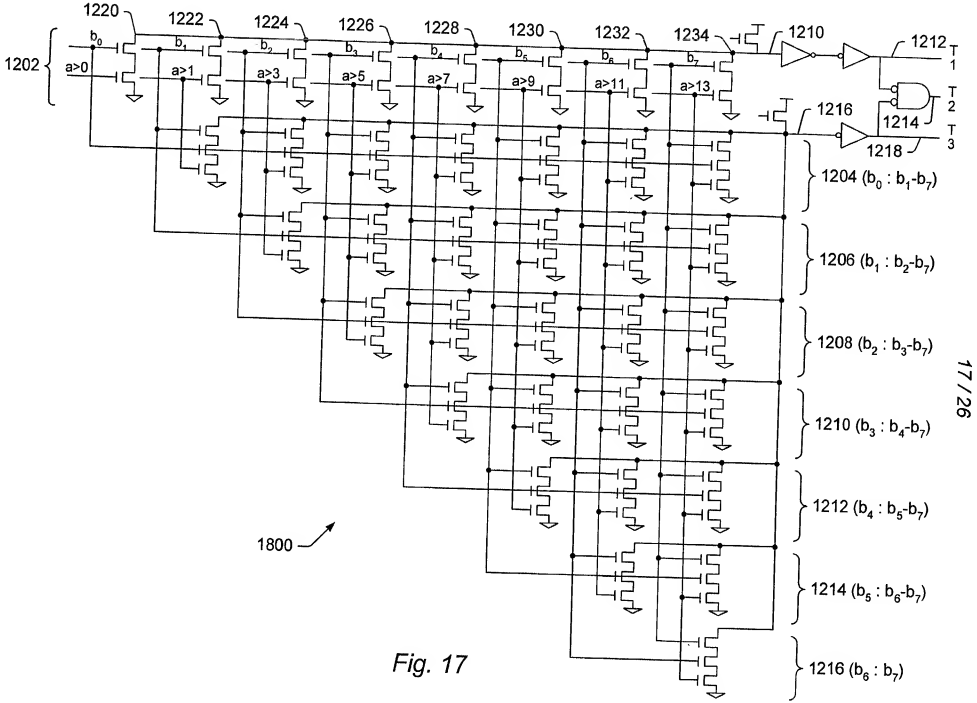

1220
1222
1224
1226
1228
1230
1232
1234
1210
1212
1202
b0
b1
b2
b3
b4
b5
b6
b7
a>0
a>1
a>3
a>5
a>7
a>9
a>11
a>13
1216
1214
1218
T1
T2
T3
1204 (b0 : b1-b7)
1206 (b1 : b2-b7)
1208 (b2 : b3-b7)
1210 (b3 : b4-b7)
1212 (b4 : b5-b7)
1214 (b5 : b6-b7)
1216 (b6 : b7)
1800

Fig. 17

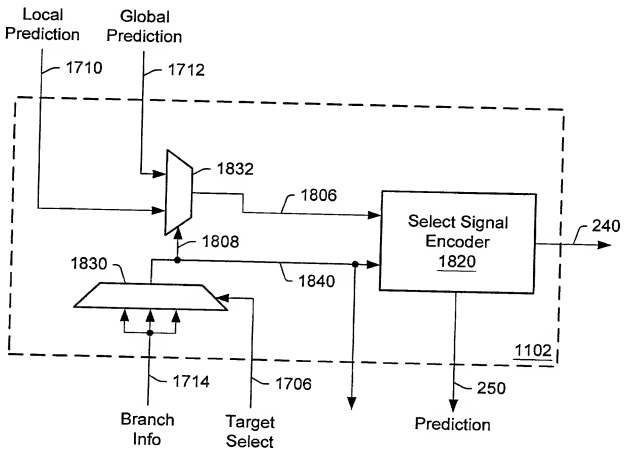

Local Prediction
Global Prediction
1710
1712
1832
1806
Select Signal Encoder
1820
240
1808
1830
1840
1102
1714
1706
250
Branch Info
Target Select
Prediction

Fig. 18

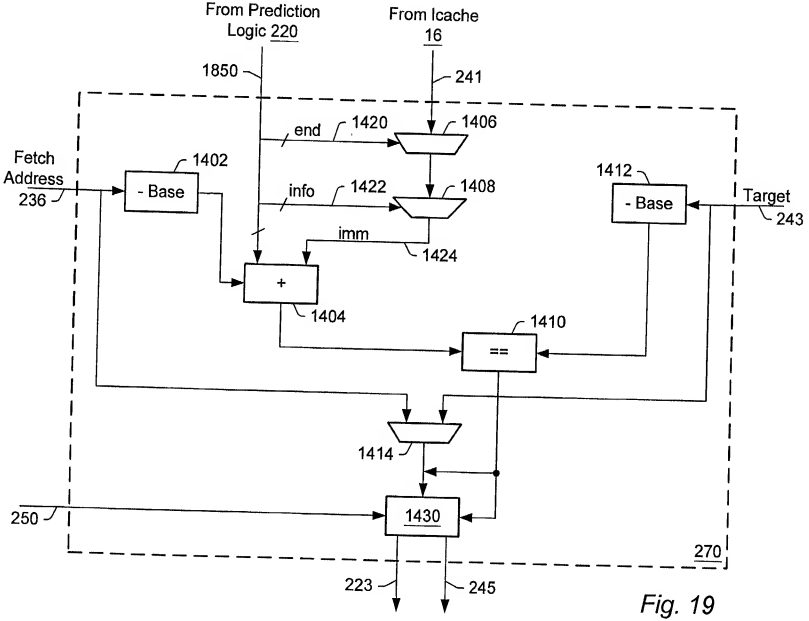

From Prediction Logic 220
From Icache 16
1850
241
end
1420
1406
Fetch Address
236
1402
- Base
info
1422
1408
1412
- Base
Target
243
imm
1424
+
1404
1410
==
1414
250
1430
270
223
245

Fig. 19

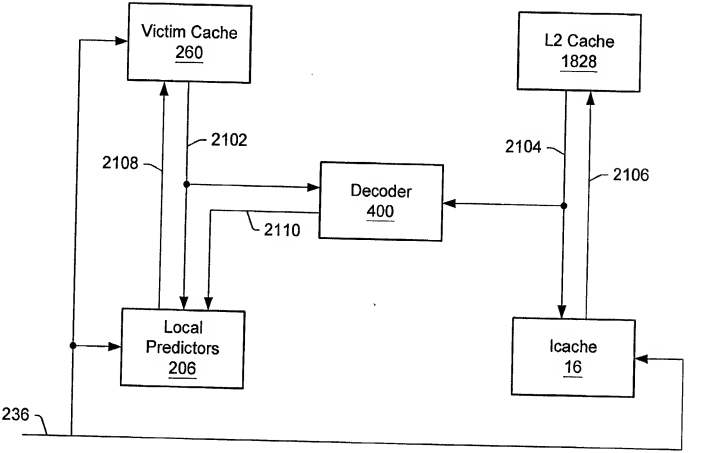

Victim Cache
260
L2 Cache
1828
2102
2104
2108
2106
Decoder
400
2110
Local
Predictors
206
Icache
16
236

Fig. 20

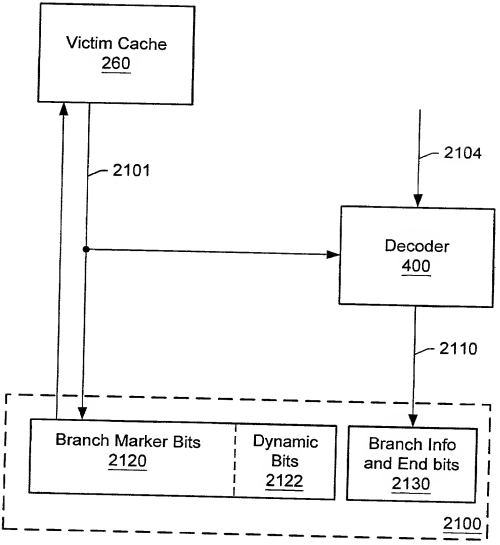

Victim Cache
260
2101
2104
Decoder
400
2110
Branch Marker Bits
2120
Dynamic
Bits
2122
Branch Info
and End bits
2130
2100

Fig. 21

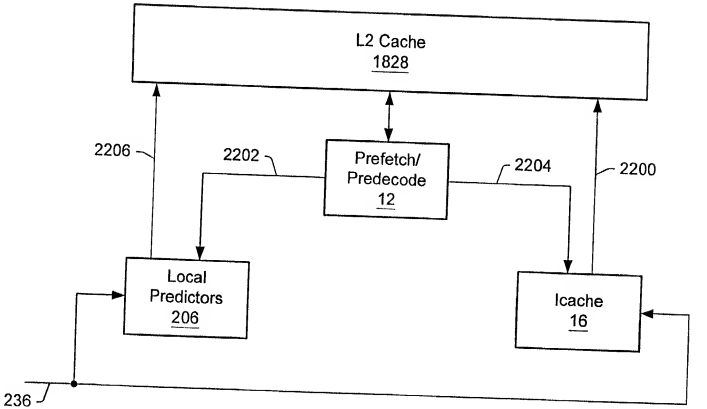
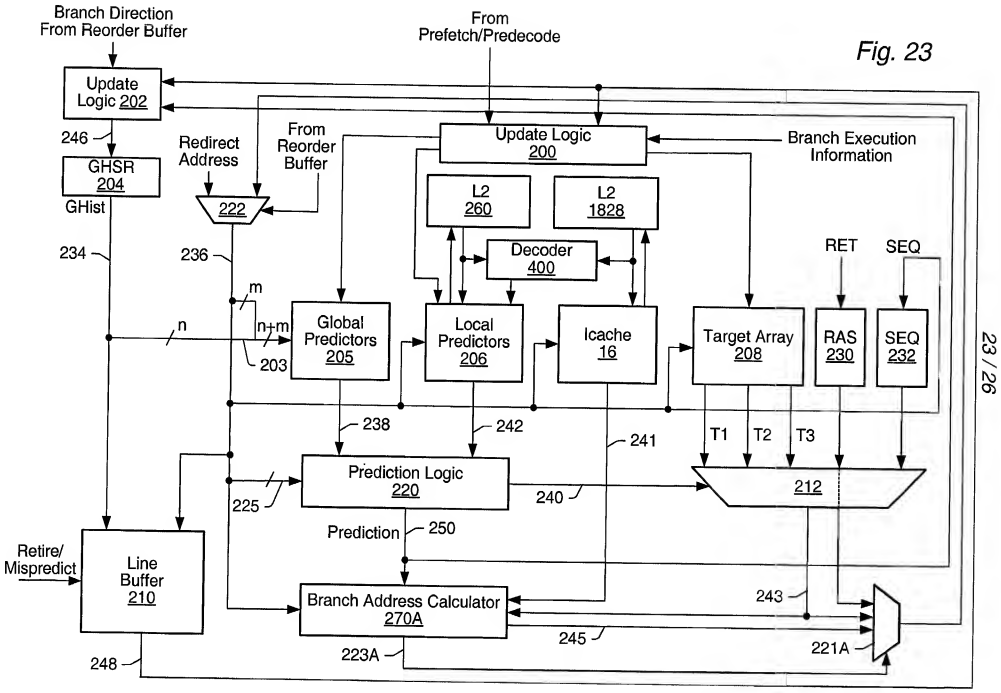

L2 Cache
1828
2206
2202
Prefetch/
Predecode
12
2204
2200
Local
Predictors
206
Icache
16
236

Fig. 22

Fig. 23


Branch Direction From Reorder Buffer
From Prefetch/Predecode
Update Logic 202
Update Logic 200
Branch Execution Information
246
GHSR 204
GHist
Redirect Address
From Reorder Buffer
222
L2 260
L2 1828
Decoder 400
RET
SEQ
234
236
m
n
n+m
203
Global Predictors 205
Local Predictors 206
Icache 16
Target Array 208
RAS 230
SEQ 232
238
242
241
T1
T2
T3
Prediction Logic 220
225
240
212
Prediction
250
Retire/ Mispredict
Line Buffer 210
Branch Address Calculator 270A
243
245
221A
223A
248

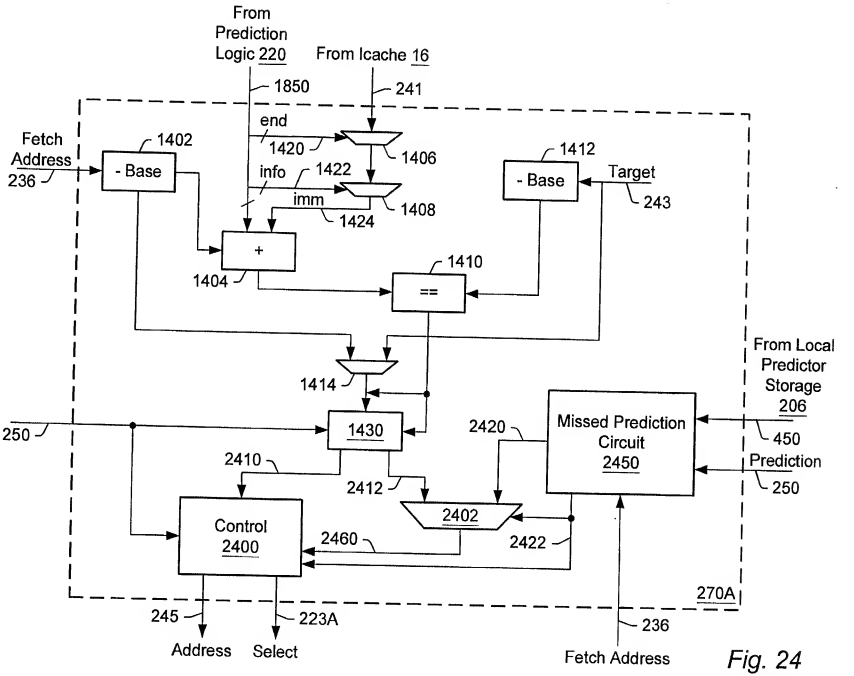

From Prediction Logic 220
From Icache 16
1850
241
end
1420
1406
info
1422
imm
1424
1408
Fetch Address
236
1402
- Base
1412
- Base
Target
243
+
1404
1410
==
1414
From Local Predictor Storage 206
250
1430
2420
Missed Prediction Circuit 2450
450
Prediction
250
2410
2412
2402
Control 2400
2460
2422
270A
245
223A
236
Address
Select
Fetch Address

Fig. 24

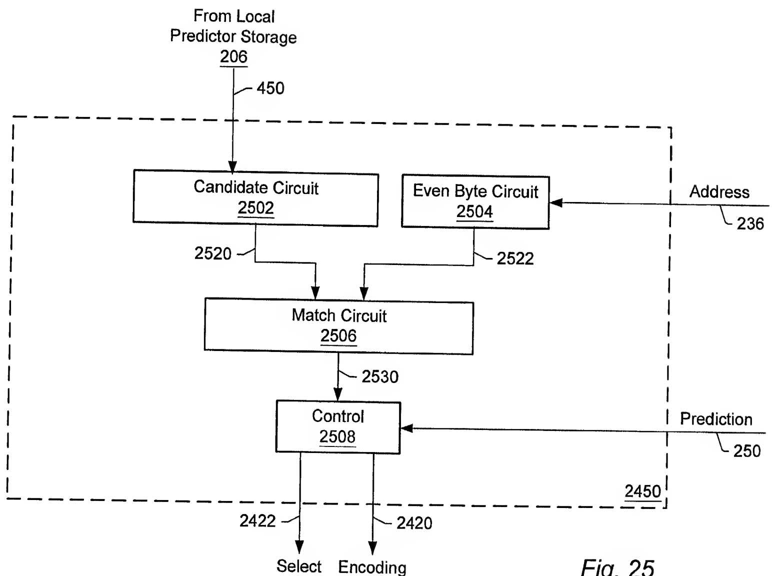

From Local
Predictor Storage
206
450
Candidate Circuit
2502
Even Byte Circuit
2504
Address
236
2520
2522
Match Circuit
2506
2530
Control
2508
Prediction
250
2450
2422
2420
Select
Encoding

Fig. 25

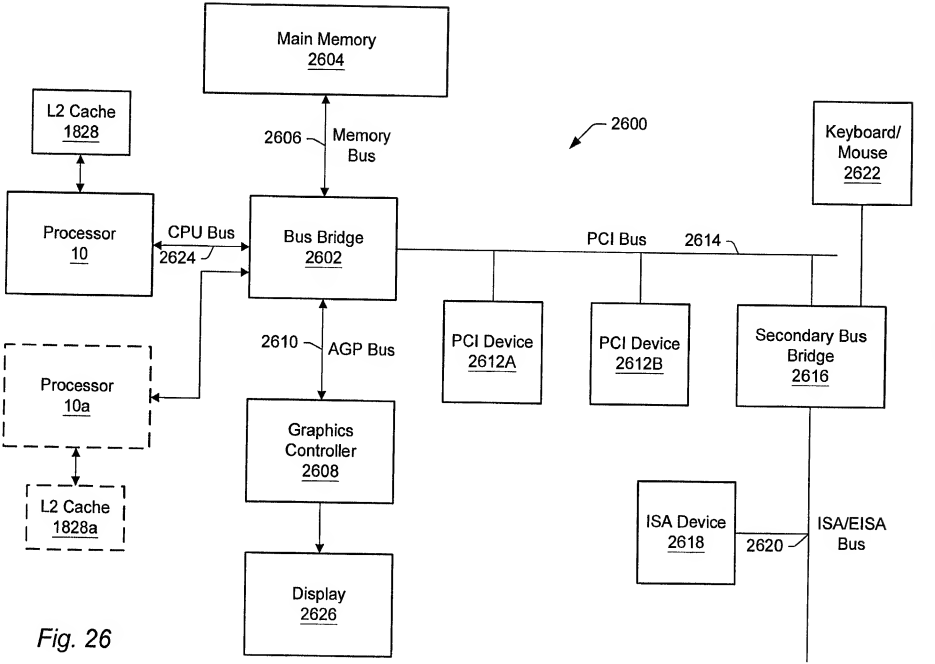

Main Memory
2604
L2 Cache
1828
2606
Memory
Bus
2600
Keyboard/
Mouse
2622
Processor
10
CPU Bus
2624
Bus Bridge
2602
PCI Bus
2614
2610
AGP Bus
PCI Device
2612A
PCI Device
2612B
Secondary Bus
Bridge
2616
Processor
10a
Graphics
Controller
2608
L2 Cache
1828a
ISA Device
2618
2620
ISA/EISA
Bus
Display
2626

Fig. 26